Parameter Variability in Nanoscale Fabrics: Bottom-Up Integrated Exploration

Pritish Narayanan[1], Michael Leuchtenburg[1], Jorge Kina[2], Prachi Joshi[1],
Pavan Panchapakeshan[1], Chi On Chui[2] and C. Andras Moritz[1]
[1]University of Massachusetts Amherst
Amherst MA 01003
[2]University of California
Los Angeles CA 90024
{pnarayan, andras}@ecs.umass.edu

Abstract

Emerging nano-device based architectures will be impacted by parameter variation in conjunction with high defect rates. Variations in key physical parameters are caused by manufacturing imprecision as well as fundamental atomic scale randomness. In this paper, the impact of parameter variation on nanoscale computing fabrics is extensively studied through a novel integrated methodology across device, circuit and architectural levels. This integrated framework enables to study in detail the impact of physical parameter variation across all fabric layers for the first time. The framework, while generic, is explored extensively on the Nanoscale Application Specific Integrated Circuits (NASICs) nanowire fabric. For key physical parameters, the on current is found to vary by up to 3.5X. Circuit-level delay shows up to 40% deviation from nominal. Monte Carlo simulations using the architectural simulator found 67% nanoprocessor chips to operate below nominal frequencies due to variation. However, given high defect rates in nano-manufacturing, built-in fault tolerance needs to be incorporated for achieving acceptable yields. These techniques are shown to also ameliorate the effects of parameter variation.

Index Terms

Semiconductor Nanowires, Parameter Variation, Device Simulation, Circuit Simulation, NASICs, Nanoscale Fabrics, Delay Characterization

I. Introduction

Emerging nano-materials and devices such as semiconductor nanowires [1], [2], carbon nanotubes [3] and molecular devices [4] have been proposed for novel computational fabrics with density and performance potentially far exceeding the capabilities of scaled CMOS. However, reliable and deterministic manufacturing of such systems continues to be very challenging. Self-assembly based approaches as well as photolithography at features sizes of few tens of nanometers and below are expected to introduce significant levels of permanent defects as well as large variations in physical parameters. While permanent defects have been extensively analyzed at circuit and system levels through approaches such as built-in defect tolerance [5], [6] and reconfiguration [7], [8], there is little understanding of the impact of parameter variability for emerging nanoscale fabrics.

Parameter variations arise due to imprecision in the manufacturing process as well as fundamental atomic scale randomness. At nanometer dimensions where structures typically consist of tens of atoms/molecules, even a small absolute variation in the number of atoms causes a large shift in the electrical characteristics (e.g., random dopant fluctuation and V_{TH} [9]). This could potentially lead to performance deterioration and/or yield loss.

In this paper, we explore the impact of variability on a nanoscale fabric. We develop a detailed methodology that is integrative across device, circuit and architectural layers. We identify key sources of variability at the physical layer, such as channel and gate dimensions of transistors and analyze how these impact electrical properties (e.g. on-currents). We then characterize delay data for circuits incorporating these devices and use them in architectural simulations to evaluate performance impact on a nanoprocessor design. While there has been some previous work in characterizing properties of nanomaterials (e.g., distributions of nanowire diameters for a particular manufacturing setup [1], [10]) and devices (e.g. on-current variation [11]), this is the first time that an integrated bottom-up approach evaluating implications of variability across multiple fabric levels is presented.

The variability framework, while fully generic, is explored extensively on the Nanoscale Application Specific Integrated Circuits (NASICs) nanowire-based computational fabric [5], [6], [12], [13], [14]. NASICs consist of semiconductor nanowire grids with crossed nanowire field effect transistors (xnwFETs) functionalized at certain crosspoints and dynamic data-streaming circuits. Built-in defect tolerance schemes provide resilience against manufacturing defects such as stuck-on xnwFETs. The NASIC WIre Streaming Processor version-0 (WISP-0) [15], [16] is a stream processor on the NASIC fabric that is used as a test case for quantifying variability (specifically performance degradation).

The main contributions of this paper are: i) A novel methodology for integrated exploration of parameter variability across nanodevice, circuit and system levels is presented; and ii) Variability effects are analyzed in detail for xnwFET devices and associated NASIC circuits and systems.

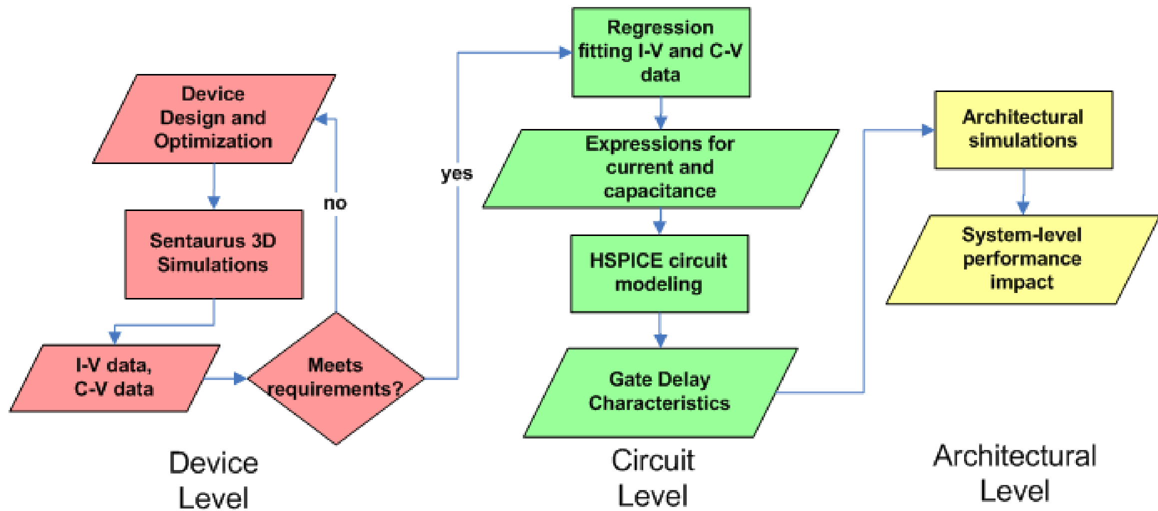

Figure 1. Methodology integrating device, circuit and architectural level explorations

The rest of the paper is organized as follows: Section II describes in detail sources of variation, variability models and a generic methodology for integrated explorations. Section III analyzes the impact of variability on xnwFET device characteristics. Section IV discusses how device and fabric variations affect NASIC dynamic circuit delays as well as WISP-0 processor performance. Section V concludes the paper.

II. Model and methodology for variability analysis

In this section we present the methodology for achieving integrated device-circuit-architectural explorations considering parameter variability. This methodology, while discussed in the context of the NASIC fabric, is fully generic and can be applied to other emerging nanoscale computational fabrics for which analytical models of device behavior considering variations are not available. This integrated approach ties physical layer variability to circuit and system level metrics such as delay and performance.

The overall methodology for integrated exploration is presented in the flowchart on Fig. 1. Devices are characterized extensively using Synopsys Sentaurus [17] to extract current-voltage and capacitance-voltage information. If the device does not meet circuit requirements for correct functionality, device design may be iteratively carried out. Otherwise, the current and capacitance data are fitted using a standard curve-fit tool to obtain mathematical expressions for the data. Using these, a unified behavioral model is created for a circuit simulator such as HSPICE [18]. The unified behavioral model accurately describes the behavior of a single device across a range of input voltages and physical parameter values. Circuit level simulations incorporating Monte Carlo analysis may then be carried out to obtain distributions of circuit delays accounting for parameter variation. This information is then used by a custom nano-architectural simulator to quantify the critical path delays and performance of large-scale designs. To our best knowledge, this framework is a first of its kind. Subsequent sections describe each phase in more detail.

A. Device-level Simulations

Crossed nanowire field-effect transistors (xnwFETs) are the active devices in NASIC designs. A typical xnwFET device structure targeting NASICs is shown in Fig. 2. In this, the top Silicon nanowire acts as the gate and modulates the conductivity of the bottom Silicon nanowire, which is the channel. In an n-type xnwFET, the gate, source and drain regions are doped n^+ and the channel is p-type. Applying a positive voltage on the gate causes inversion in the p-region creating an n-type channel. A thin layer of high-permittivity (high-k) dielectric material (HfO_2) separates the gate from the channel.

Key sources of variability for a single device were identified to include channel diameter and doping, gate oxide thickness, gate diameter as well as source-drain doping. Variations in these parameters are dependent on the specific fabrication process used. For example, if a Vapor-Liquid-Solid (VLS) growth method [1] is assumed for nanowire growth, the gate and channel diameter parameters would be very strongly correlated to variations in the catalyst nanoparticles used as seeds. The standard deviation in wire diameter has been shown to be around 10% in [1], [10]. The ITRS roadmap [19] defines the extent of variability allowed for key parameters. For example, gate oxide is constrained to vary by 3σ=4%. Other process parameters are similarly tightly constrained.

For NASIC system fabrication, different approaches are currently being investigated; e.g., nanowire growth and alignment may be done *in-situ* [20], [21], [22] or *ex-situ* [23], [24], [25]. Similarly, ion implantation or spin-on-dopants [26] may be used

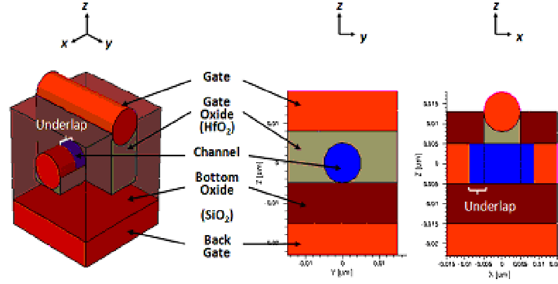

Figure 2. Crossed Nanowire Field Effect Transistor (xnwFET) structure

Table I
DEVICE PARAMETERS AND EXTENT OF VARIATION

Parameter	Nominal Value	Standard Deviation
Channel diameter (Cdiam)	10nm	10%
Gate diameter (Gdiam)	10nm	10%
Underlap (Ulap)	4nm	10%
Gate oxide thickness (Gox)	3nm	10%
Bottom oxide (Box)	10nm	10%
Channel doping (Cdop)	$10^{18} dopants/cm^3$	10%
Source-drain doping (Sddop)	$10^{20} dopants/cm^3$	10%

for doping process. Therefore, for our initial variability modeling, we conservatively model 10% standard deviation (3σ=$\pm$30%) for all parameters to capture worst case scenarios. As more experimental data on device characterization becomes available and detailed process models developed, the extent of variation can be suitably altered.

xnwFETs need to be engineered to meet NASIC circuit requirements (e.g., threshold voltage, on-off current ratios [13]). Device level techniques such as gate underlap and substrate bias were applied in conjunction to achieve these targets. However, these techniques can be sources of additional variability. For example, applying a potential at the substrate implies that the electrostatic behavior is sensitive to the bottom oxide thickness, in addition to the top gate oxide. Similarly, variation in the length of the underlap can significantly affect I-V characteristics. Table I summarizes all parameters and their extent of variability.

Accurate 3D-physics-based simulations using Synopsys Sentaurus were carried out to characterize the electrical behavior of the xnwFET device structure. Simulations were calibrated against published experimental data for nanowire FETs at similar dimensions to account for effects such as carrier scattering due to surface roughness and dielectric/channel interface trapped charges. Parameters are expected to be uncorrelated since they would be influenced by separate process steps. For example, the gate oxide may be created using Atomic Layer Deposition (ALD) [27]. While there will be spatial variability on a wafer due to ALD (which is the source of variation for the device), there is no dependence of this parameter on any other. Similarly, variation in the underlap is purely dependent on the spacers used, and not on any other step. Therefore, to this end, in these simulations, each parameter was varied one at a time for $\pm 3\sigma$ and the I-V and C-V data were obtained for all device configurations. This data was then used to construct unified behavioral models for circuit simulations.

B. Circuit-level simulations

In order to represent the behavior of the device accurately in a circuit simulator such as HSPICE [18], curve-fitting of the raw data obtained from device simulations needs to be done. In this step, the current (and various parasitic capacitances) are fitted as a function of independent variables, i.e., input voltages (drain-source (V_{DS}) and gate-source voltages (V_{GS})) as well as the physical parameters described in Table I. This step was accomplished using the statistical computing tool R [28]. Mathematical expressions describing the current (and capacitances) as functions of the independent variables are then obtained for various regions (see Fig. 1 for flow).

An equivalent circuit for the xnwFET was then built into HSPICE incorporating the current source and the parasitic capacitances using sub-circuit definitions. The current and capacitance are calculated on-the-fly during simulations using the fitted mathematical expressions. The subcircuit definition in conjunction with the expressions for individual elements forms the unified behavioral model for the xnwFET device.

NASIC dynamic circuits were extensively characterized for delay using these models. A typical NASIC dynamic circuit is shown in Fig. 3. It has N inputs, as well as control xnwFET devices for precharge and evaluate. The output node is first precharged to logic '1', and then the *pre* signal is switched off and *eva* is enabled. If all inputs are logic '1', the output node

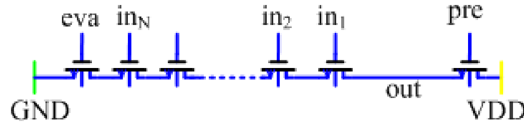

Figure 3. N-input dynamic NAND circuits characterized for delay distribution

Table II
IMPACT OF PHYSICAL PARAMETERS ON DEVICE ON-CURRENT

Parameter	% Change in I_{ON}	Correlation
Channel diameter	352.0	Positive
Underlap	181.2	Negative
Bottom oxide thickness	147.2	Positive
Gate oxide thickness	58.2	Negative
Source/drain doping	23.8	Positive
Gate diameter	16.2	Negative
Channel doping	11.7	Positive

will discharge to logic '0' accomplishing NAND gate functionality. The NAND gate is the universal building block for large scale designs, and its delay behavior needs to be extensively characterized for use in an architectural level simulator.

Delay characterization is done using NASIC dynamic NAND gates with number of inputs varying from 1 to 30. The Monte Carlo simulation framework available with HSPICE was used to vary parameter values and the delay to precharge and evaluate the output node was obtained. Parameters are assumed to follow a Gaussian distribution, with the mean and standard deviation values specified in Table I. They are varied independently for each device, except for the channel diameter which is assumed to be the same across all devices, since all devices are along the same nanowire. Since it may be very hard to do detailed circuit-level simulations on a larger design such as the WISP-0 processor, the delay information is abstracted and used in a higher level architectural simulator.

C. Architectural Simulations

The architectural simulations take as input the gate delay characterizations as shown in Fig. 1. We use a custom-written simulator called FTSIM. FTSIM takes as input a NASIC circuit definition, gate timing characterizations, and parameters for defects and simulates the operation of the circuit on a cycle-by-cycle basis, tracking values within the circuit logically.

FTSIM handles both parameter variations and permanent defects.For permanent defects, the user specifies the type of defects (e.g. stuck-on, stuck-off devices, broken nanowires) and individual defect rates. A Monte Carlo system is used for defect injection and multiple trials carried out. Clustered defects may also be handled. Additional information on defect tolerance and models can be found in [5], [6], [15].

For parameter variations, timing characterizations of NAND gates from HSPICE are used. Gate delay for any one stage is chosen from the distribution of delays obtained from circuit simulation for each trial and the maximum frequency at which correct outputs are obtained is found.

In this work, we ran 1,000 trials which produces sufficient working circuits to give a sound idea of the performance distributions. The output of this stage is the performance distributions for the test architectures considered.

III. VARIABILITY IMPACT ON XNWFET DEVICES

At the device level, variation in physical parameters affects the on-current (I_{ON}) of the device[1]. This implies variation in the on-resistance leading to variations in delay and performance at higher levels.

In this study, physical parameters from Table I are varied one at a time, and the sensitivity of I_{ON} to parameter variation is measured. Parameters are varied across a $\pm 3\sigma$ range, assuming 10% standard deviation (i.e., parameters are varied from 70% to 130% of their nominal value).

Not all parameters have equal impact on I_{ON}. The percentage change in on-current between the lowest and highest sampled value for each physical parameter is shown in Table II. Channel diameter has the largest impact, with I_{ON} varying by 3.5X over a 7nm to 13nm range.

For four parameters, positive correlation exists between the parameter value and I_{ON}. For example, as bottom oxide thickness increases, I_{ON} increases. The substrate bias is used to deplete carriers in the channel for reducing leakage and improving

[1]Off-currents are also affected, but this is primarily a leakage issue. While variation in the off-currents is captured in device simulations and in the circuit level model, it is not expected to affect the delay and performance of NASIC designs that is the focus of this paper.

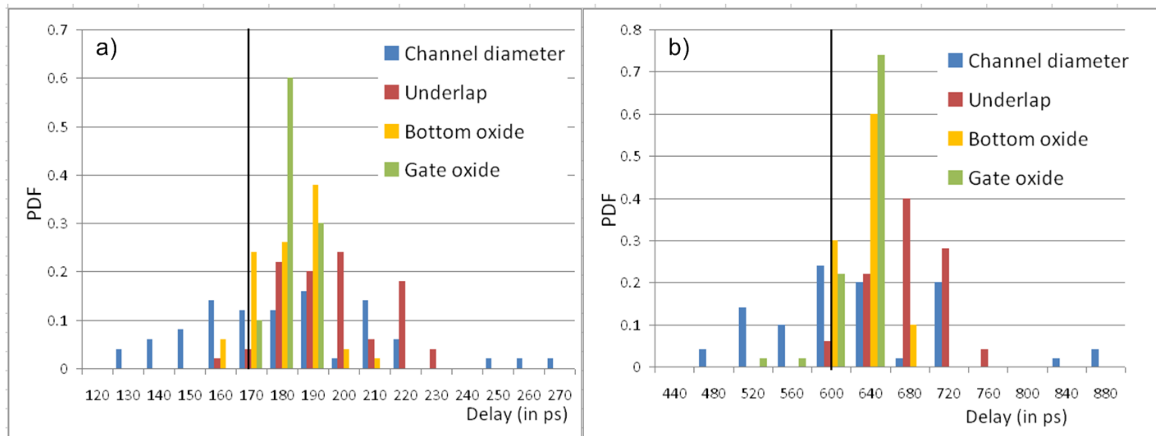

Figure 4. Delay distributions for physical parameters with maximum impact on on-current for (a) 15 input and (b) 30 input NASIC dynamic NAND gates. Black line represents nominal.

threshold voltage. However, the substrate bias also reduces I_{ON} due to a shift in the threshold voltage. As the bottom oxide is made thicker, the electrostatic control exerted by the back gate bias is reduced, producing a smaller positive V_{TH} shift than expected, leading to larger I_{ON}. As channel diameter increases, the channel resistance decreases due to an increase in the cross-sectional area, leading to an increase in I_{ON}. Increasing the source and drain doping reduces the series resistance. Lastly, as channel doping increases, the short channel effects (SCE) are somewhat alleviated leading to larger I_{ON}. The other parameters all correlate negatively with on current. Increasing the underlap increases the effective channel length, resulting in a decrease in $I_{ON.}$ Similarly, increasing the gate oxide thickness decreases the gate capacitance and how well the gate can turn on the channel. Increasing gate diameter increases the length of the channel underneath, decreasing $I_{ON.}$

IV. Variability Impact on Circuit Level Delay and System Performance

A. Circuit Level Delay Characterization

NASIC N-input dynamic NAND gates (Fig. 3) were simulated in HSPICE using unified behavioral models derived from device data. Delay characterization was done for fan-in varying between 1 and 30, which is the maximum fan-in for the NASIC WISP-0 processor, using the HSPICE Monte Carlo framework and Gaussian sampling of individual parameters. A single channel diameter value was sampled per Monte Carlo simulation for all devices, since all xnwFETs are on the same nanowire. Length-wise variation has been shown to be negligible for the nanowire lengths considered [29] for a process such as VLS growth. All other parameters were varied independently for each device.

The delay sensitivity of NASIC N-input dynamic gates to individual parameters was studied. We show the impact on delay for the four parameters that have maximum impact on I_{ON} at the device level. Representative results for fan-in of 15 and 30 are shown. Other fan-in gates were investigated and found to show similar trends.

Fig. 4(a) and (b) show the delay distributions for 15 input and 30 input NASIC dynamic NAND gates. The delay distribution due to channel diameter, underlap, bottom oxide and gate oxide thickness is studied. The following key observations are made -

Channel diameter has the maximum impact on delay distribution - 81% (71%) change in delay with respect to nominal for 15 (30) input gate. This is due to the high sensitivity of I_{ON} at the device level, and also due to the correlation of channel diameter across all devices for a single NASIC dynamic NAND circuit. These effects also imply a large percentage standard deviation - 18% (15%) for 15 (30) input gates - leading to a wide spread of delay values.

Underlap is negatively correlated with I_{ON}. This implies that delays will be less than nominal for shorter underlaps. Furthermore, from device level sensitivity analysis I_{ON} variation is asymmetrical with underlap. 30% negative (positive) deviation causes +74% (-43%) change in the I_{ON}. This would imply that in a circuit simulation, where underlap values for individual devices are independently sampled, the delay distribution should be left-shifted (majority of devices operating better than nominal). However, the opposite trend is noticed. This is because increasing trend in the I_{ON} with decreasing underlap is dominated by an increasing trend in the various capacitances as distances between terminals shrink.

The evaluation delays for **gate oxide** and **bottom oxide** are tightly distributed along the nominal, with mean values within 2% of nominal and standard deviation of 3% for the 30 input gate. Since these parameters are sampled independently, and there exist no appreciable asymmetries as compared to the underlap, variation in delays of individual devices tend to cancel out especially in higher fan-in designs.

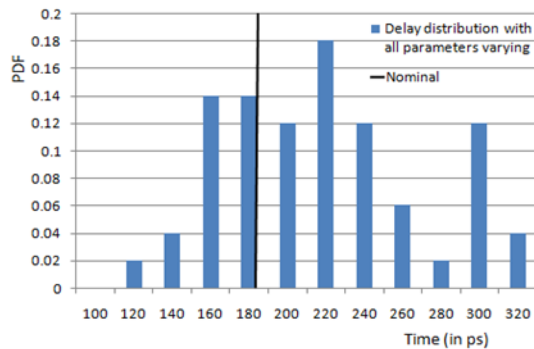

Figure 5. Delay distribution for 15 input gate with all parameters simultaneously varied: Nominal value is 174ps. Distribution is right-shifted due to asymmetric underlap effect

Fig. 5 shows delay distributions for the 15 input NASIC dynamic NAND gate with all parameters varied simultaneously with 3σ=±30%. The mean is 20% higher than the nominal due to the underlap asymmetry effect that skews the distribution to the right. The same trend is observed in other fan-in gates as well. A 118% spread with respect to the nominal is observed for 15 input gates. The relative spread was found to be decreasing with increasing fan-in, as expected.

The gate delay distributions with all parameters varying for different fan-ins were modeled as gamma distributions and used in an architectural simulator to evaluate the process variation impact on a larger design.

B. System Level Performance

Architectural simulations of the NASIC WISP-0 processor [15], [16] were carried out using the architectural simulation framework described in Fig. 1 and Section II-C. Gate delay distributions obtained from Monte Carlo simulations of NASIC dynamic NAND gates were sampled for each gate in the design and the maximum operating frequency at which the processor functioned without missed deadlines was estimated.

The probability density function of operating frequencies obtained is plotted in Fig. 6(a). Also shown in the diagram is the nominal frequency for WISP-0 without any process variation. (Note: performance optimizations on device structure are currently ongoing - while we expect future devices to be considerably faster and thus the processor performance would be also much improved, it would not change the conclusions qualitatively). From the diagram, parameter variation causes performance deterioration in 67% of the samples investigated.

WISP-0 is not fully balanced with respect to timing and delay. The frequency is therefore determined entirely by a small number of high fan-in data-paths. If the delays sampled from these paths are lower than nominal then the performance of the entire design is not affected or may even improve. However, in designs balanced for timing, such as commercial processors where a lot of emphasis is typically put on timing path optimizations, there will be a large number of paths with similar nominal delay. The slowest path among these would determine the operating frequency. This implies that for balanced designs with process variation, a much larger fraction of chips will be slower than nominal, since data speed-up along some high fan-in paths will be entirely offset by others.

Results in Fig. 6(a) are for designs with no built-in fault tolerance. However, nanoscale fabrics based on self-assembly manufacturing processes tend to have very high defect rates (in NASICs we assume 10 orders of magnitude higher than CMOS or 100s of millions to billions of defective devices per cm^2) that neccessitates the use of built-in fault tolerance for achieving acceptable effective yield. These techniques may also provide resilience against parameter variation related timing faults, since the fault-tolerance is agnostic to the source of the fault (permanent defects or parameter variation) and may be leveraged for parameter variation resilience.

Fig. 6(b) plots a distribution of maximum operating frequencies obtained for 2-way and 3-way redundant WISP-0 designs for 6% device level defect rate. The x-axis is normalized to the respective nominal frequencies (no parameter variation). In these cases, timing faults due to slower data-paths are masked by redundant fast data-paths which implies that a majority of samples (75% for 2-way redundancy) operate at frequencies better than nominal, proving that built-in fault tolerance can provide resilience against parameter variations in conjunction with manufacturing defects. A variety of new techniques carefully managing yield and performance tradeoffs and optimized for parameter variation as opposed to permanent defects are currently under investigation for nanoscale fabrics.

V. Conclusions

A novel methodology for bottom-up integrated device-circuit-architectural explorations for analyzing the impact of parameter variability in nano-device based computing systems was developed. The methodology builds on accurate 3D physics based

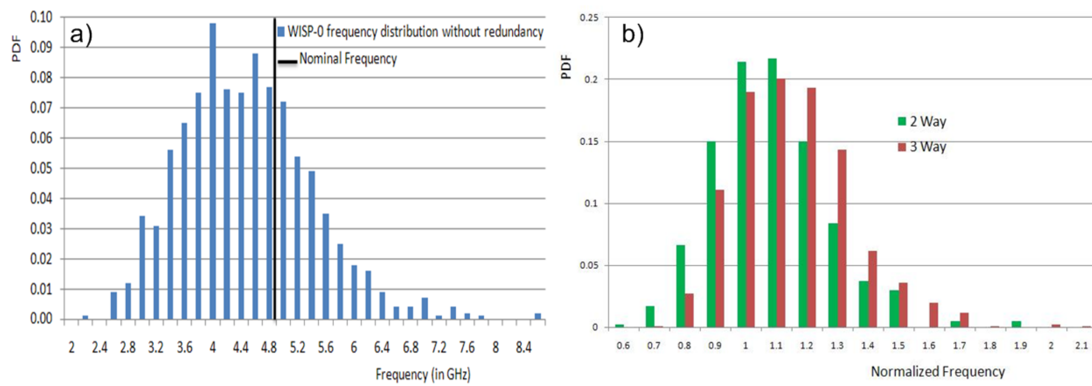

Figure 6. Distribution of WISP-0 operating frequencies showing impact of parameter variations: (a) With no built-in fault tolerance incorporated, 67% of chips operate at frequency below nominal due to variations in device parameters (b) PDF for 2-way and 3-way redundancy schemes, showing a majority of samples operating at better-than-nominal frequencies (normalized frequency > 1).

simulations of device structure to capture variations in on-current as a function of physical parameters. Circuit and architectural simulations evaluate the impact of this variability on gate delay and system level performance respectively.

The methodology was evaluated on the NASIC computational fabric with xnwFETs, NASIC dynamic NAND gates and a processor design. Key sources of variation at the device level such as channel diameter were identified and sensitivity of I_{ON} was evaluated. I_{ON} may vary by up to 3.5X with variations in the channel diameter and by up to 1.5X with gate underlap. Circuit level simulations identified the evaluate time in NASIC designs as the dominant component of the gate delay with parameter variation incorporated. Gate delay simulations varying a single parameter show up to $\pm 40\%$ variation from nominal gate delay.

For a processor with no fault tolerance, 67% of chips were found to operate at frequencies below nominal due to parameter variation. However given high defect rate for nanomanufacturing, nanoscale computing fabrics would incorporate built-in fault tolerance that could also provide resilience against timing faults.

Acknowledgment

This work was supported in part by the Focus Center Research Program (FCRP) Center on Functionally Engineering Nano Architectonics (FENA), the Center for Hierarchical Manufacturing (CHM) at UMass Amherst, and NSF awards CCR:0105516, NER:0508382, and CCR:051066.

References

[1] W. Lu and C. M. Lieber, "Semiconductor nanowires," *Journal of Physics D: Applied Physics*, vol. 39, no. 21, pp. R387–R406, 2006.
[2] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, "Doping and electrical transport in silicon nanowires," *The Journal of Physical Chemistry B*, vol. 104, no. 22, pp. 5213–5216, Jun. 2000.
[3] Z. Chen, J. Appenzeller, Y. Lin, J. Sippel-Oakley, A. G. Rinzler, J. Tang, S. J. Wind, P. M. Solomon, and P. Avouris, "An integrated logic circuit assembled on a single carbon nanotube," *Science*, vol. 311, no. 5768, p. 1735, Mar. 2006.
[4] C. P. Collier, E. W. Wong, M. Belohradsk, F. M. Raymo, J. F. Stoddart, P. J. Kuekes, R. S. Williams, and J. R. Heath, "Electronically configurable Molecular-Based logic gates," *Science*, vol. 285, no. 5426, pp. 391–394, Jul. 1999.
[5] T. Wang, P. Narayanan, and C. A. Moritz, "Heterogeneous Two-Level logic and its density and fault tolerance implications in nanoscale fabrics," *IEEE Transactions on Nanotechnology*, vol. 8, no. 1, pp. 22–30, 2009.
[6] C. Moritz, T. Wang, P. Narayanan, M. Leuchtenburg, Y. Guo, C. Dezan, and M. Bennaser, "Fault-tolerant nanoscale processors on semiconductor nanowire grids," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, no. 11, pp. 2422 –2437, nov. 2007.
[7] D. B. Strukov and K. K. Likharev, "Reconfigurable hybrid CMOS/Nanodevice circuits for image processing," *IEEE Transactions on Nanotechnology*, vol. 6, pp. 696–710, Nov. 2007.
[8] G. S. Snider and R. S. Williams, "Nano/CMOS architectures using a field-programmable nanowire interconnect," *Nanotechnology*, vol. 18, no. 3, p. 035204, 2007.
[9] H. P. Wong, Y. Taur, and D. J. Frank, "Discrete random dopant distribution effects in nanometer-scale MOSFETs," *Microelectronics and Reliability*, vol. 38, no. 9, pp. 1447–1456, Sep. 1998.
[10] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Applied Physics Letters*, vol. 78, no. 15, p. 2214, 2001.
[11] S. R. Mehrotra and K. Roenker, "Process variation study for silicon nanowire transistors," *Microelectronics and Electron Devices, 2007. WMED 2007. IEEE Workshop on*, pp. 40–41, 2007.
[12] P. Narayanan, M. Leuchtenburg, T. Wang, and C. A. Moritz, "CMOS control enabled Single-Type FET NASIC," in *Proceedings of the 2008 IEEE Computer Society Annual Symposium on VLSI*. IEEE Computer Society, 2008, pp. 191–196.
[13] P. Narayanan, C. A. Moritz, K. W. Park, and C. O. Chui, "Validating cascading of crossbar circuits with an integrated device-circuit exploration," in *Nanoscale Architectures, IEEE International Symposium on*. IEEE Computer Society, 2009, pp. 37–42.
[14] P. Narayanan, K. W. Park, C. O. Chui, and C. Moritz, "Manufacturing pathway and associated challenges for nanoscale computational systems," in *Nanotechnology, 2009. IEEE-NANO 2009. 9th IEEE Conference on*, 26-30 2009, pp. 119 –122.

[15] T. Wang, M. Ben-naser, Y. Guo, and C. A. Moritz, "Wire-streaming processors on 2-D nanowire fabrics," *NANOTECH 2005, NANO SCIENCE AND TECHNOLOGY INSTITUTE*, 2005.
[16] T. Wang, P. Narayanan, and C. A. Moritz, "Combining 2-level logic families in grid-based nanoscale fabrics," in *Proceedings of the 2007 IEEE International Symposium on Nanoscale Architectures*. IEEE Computer Society, 2007, pp. 101–108.
[17] "Sentaurus device user guide," 2007, synopsys, Inc.
[18] "Hspice user's manual," 2007, synopsys, Inc.
[19] "International technology roadmap for semiconductors (itrs)," 2007. [Online]. Available: http://public.itrs.org
[20] R. He, D. Gao, R. Fan, A. I. Hochbaum, C. Carraro, R. Maboudian, and P. Yang, "Si nanowire bridges in microtrenches: Integration of growth into device fabrication," *Advanced Materials*, vol. 17, no. 17, pp. 2098–2102, 2005.
[21] Y. Shan and S. J. Fonash, "Self-Assembling silicon nanowires for device applications using the Nanochannel-Guided Grow-in-Place approach," *ACS Nano*, vol. 2, no. 3, pp. 429–434, Mar. 2008.
[22] A. Ural, Y. Li, and H. Dai, "Electric-field-aligned growth of single-walled carbon nanotubes on surfaces," *Applied Physics Letters*, vol. 81, no. 18, p. 3464, 2002.
[23] D. Whang, S. Jin, and C. M. Lieber, "Nanolithography using hierarchically assembled nanowire masks," *Nano Letters*, vol. 3, no. 7, pp. 951–954, Jul. 2003.
[24] X. Xiong, L. Jaberansari, M. G. Hahm, A. Busnaina, and Y. J. Jung, "Building highly organized Single-Walled-Carbon-Nanotube networks using Template-Guided fluidic assembly13," *Small*, vol. 3, no. 12, pp. 2006–2010, 2007.
[25] Y. Liu, J. Chung, W. K. Liu, and R. S. Ruoff, "Dielectrophoretic assembly of nanowires," *The Journal of Physical Chemistry B*, vol. 110, no. 29, pp. 14 098–14 106, Jul. 2006.
[26] D. Wang, B. Sheriff, M. McAlpine, and J. Heath, "Development of ultra-high density silicon nanowire arrays for electronics applications," *Nano Research*, vol. 1, no. 1, pp. 9–21, Jul. 2008.
[27] M. Ritala and M. Leskela, "Atomic layer deposition," *High-K Gate Dielecrics*, pp. 17–64, 2004.
[28] "The r project for statistical computing." [Online]. Available: http://r-project.org
[29] W. I. Park, G. Zheng, X. Jiang, B. Tian, and C. M. Lieber, "Controlled synthesis of Millimeter-Long silicon nanowires with uniform electronic properties," *Nano letters*, vol. 8, no. 9, pp. 3004–3009, Sep. 2008.