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**Electrical Engineering Department Colloquium  
FENA Seminars**

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Title

**Youssry Botros**

Intel Corporation

**Thursday, March 3rd, 2005**

**8500 Boelter Hall (Penthouse)**

**4:00 pm - 5:30 pm**

*Refreshments will be served*

**Abstract**

With the introduction of silicon nano-technology, feature sizes are shrinking and as a result, smaller variations will adversely affect product quality, yield and cost. To minimize variability, Process Control is applied to prevent excursions, improve yield, decrease non-product runs, reduce cycle time due to rework, and reduce equipment calibration and maintenance. Process Control Systems (PCS) are designed and deployed to achieve the desired levels of process tightening. Intel PCS involve rapid detection, classification, prediction, and correction of problems and non-optimal performance during wafer manufacturing. These PCS capabilities are implemented via several systems, namely Run-to-Run (R2R) control, Fault Detection and classification (FDC), and statistical Process Control (SPC). For efficient process control, a robust analysis is needed in order to monitor the process effectively, detect, and predict the process behavior. The presentation will address Intel model based control applications and will focus on the various model based analysis and control modules that Intel has developed, and deployed for different technology generations.

The aforementioned PCS need to be efficiently integrated to achieve the desired level of process specifications and such integration can be achieved through consistent functional grouping, architectural alignment and standardized interfaces. Intel PCS integration is a part of an overall strategy implemented to allow efficient automation support for process technology development. Integrated automation FW architecture is being developed and deployed to Intel newest Fab, located at Hillsboro, Oregon. This Fab (D1D) started the production of 65nm node wafers. Achieving integration goals will require conformance to industry interface standards. Open, standardized interfaces are required to avoid custom solutions, which increase implementation time with an added cost to both IC makers and suppliers. Intel is leading the development of PCS interfaces that enable PCS to interact effectively and share data among themselves and other factory systems. The PCS SEMI standards ballot was approved in 2003 and this industry consensus is a major milestone that will enable the integration.

**Biography:**

Youssry Botros is a staff Engineer with the Technology Strategy Group, Intel Corporation. He obtained his Ph.D. from the University of Michigan, Ann Arbor in 1998. His research focused on applying computational methods to solve large scale problems such as antenna and electromagnetic structures, high intensity frequency focused ultrasound arrays for cancer ablation, and vehicle electromagnetic Interference analysis. He joined the Logic Technology Department (LTD) at Intel Corporation in 1999 where he worked in developing Lithography algorithms and modules that analyzes metrology (overlay and Registration) data to determine the health of the patterning processes and take pass/fail/rework decisions on the material. After that, he managed the Process Control Systems (PCS) Architecture team that developed and currently implementing the Integrated PCS Architecture at Intel. He chaired the International SEMI Process Control Systems that developed the E133 SEMI Standard approved in 2003. Also, he managed several LTD projects in the areas of Lithography, Advanced Design (Tape Out) and Process Control. Currently is Intel's resident at the FENA Center at UCLA.

The speaker may be contacted directly at: [Youssry.y.botros@intel.com](mailto:Youssry.y.botros@intel.com)

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*For additional information please see the Colloquium web page: [www.ee.ucla.edu/colloquium](http://www.ee.ucla.edu/colloquium)  
or contact Professor Lei He ([lhe@ee.ucla.edu](mailto:lhe@ee.ucla.edu))*

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**Future UCLA Electrical Engineering Department Colloquia: April 7, May 5, and June 2. Please mark your calendar!**

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