



A forum on the Frontiers in Computational Nanoelectronics

Date: February 20-21, 2007
Location: University Place, Indianapolis, IN

Hosted by the Network Computational Nanotechnology (NCN)
Organized by NCN and:
SRC, MARCO, and NRI
MSD and FENA Focus Centers
WIN, INDEX, and SWAN NRI Centers

This small, informal workshop designed to:

- 1) Promote communication and identify opportunities for collaboration between SRC, MARCO, and NRI-funded university researchers working on theory, modeling, and simulation of ultimate CMOS, CMOS plus, and beyond CMOS devices.
- 2) Identify key challenges in modeling and simulation for the SRC, MARCO, and NRI programs and to identify promising solutions.
- 3) Provide experimental collaborators and industrial partners with a bird's eye view of the current status of university research.
- 4) Provide a forum to communicate industry / sponsor needs to university researchers and to identify mechanisms to promote industry- university collaboration.
- 5) Encourage the use of NCN software/middleware and collaboration technology.



Who should attend?

SRC, MSD, FENA, WIN, INDEX, SWAN faculty engaged in theory, modeling, and simulation of advanced electronic devices.

Other PI's and industrial partners of these centers interested in a broad overview at what's happening nationwide in theory, modeling, and simulation

Attendance is limited to 75 academic / industry participants from SRC, MARCO-MSD, MARCO-FENA, and NRI programs: see:

http://www.NCN.purdue.edu/workshops/frontiers_in_computational_nanoelectronics