Title: Nanodevice Array for Digital Logic Using One-Dimensional Functional Nanomaterials
Speaker: H.-S. Philip Wong (Stanford University)
Student: Jie Deng (Stanford University)
Date: Thursday, January 6th
Time: 3:00 PM (Pacific), 6:00 PM (Eastern)

Limited seating available: Please RSVP to Katie Christensen at Katie@fena.org if you plan on attending.

ABSTRACT

Nanoscale devices (cross-point molecular diodes and nanowire/nanotube FETs) can be arranged in a crossbar array. This architecture has been proposed as ultra-high density nanoscale systems requiring only simple fabrication processes based on self-assembly [i]. To achieve ultra-high device density, the nanodevice array can be made with a sub-lithographic half-pitch (F_S) smaller than the general lithographic half-pitch (F) using self-assembly or other chemical synthesis methods. Self-assembly methods usually lead to regularly organized structures. Configuring nanodevices on a regular grid may be the only way to fabricate nanodevices with densities beyond the lithographic limit.

The overarching goal of this project at FENA is to analyze the system benefits of the nanodevice array architecture, and experimentally demonstrate a working nanodevice array using one-dimensional functional nanomaterials investigated in the FENA MARCO Focus Center.

In this talk, we will review the progress of this project in the past 5 months. We developed a new SPICE (circuit simulator) compatible device model for the analysis of circuit performance of CNFET. The model takes into account the essential physics of the CNT including band structure effects. The performances of CNFET random logic were compared to 32 nm node CMOS random logic using Digital Standard Library circuits. Practical layout patterns of CNFET circuits were considered including all the parasitic capacitances due to wiring. The minimum design rules were applied to CMOS circuits to minimize the Energy-Delay-Product (EDP). The effects of multiple CNTs per device were also investigated. A sub-lithography pitch F_s which can be much finer than lithography pitch F can be obtained with self-assembly process without increasing the cell area. For a variety of circuits, the delay of CNFET circuits is about 2-20X lower than that of CMOS circuits, the energy per cycle of CNFET circuits is about 2-10X lower than that of CMOS circuits, and the EDP of CNFET circuits is about 20-50X lower than that of CMOS circuits.

[i] A. DeHon, "Array-Based Architecture for FET-Based, Nanoscale Electronics," ***IEEE Trans. Nanotechnology*****, pp. 23 – 32 (2003).**

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