



**Forum on:  
FENA Memory and Nanopatterning Projects**

January 30<sup>th</sup> – LUXE Hotel  
“Malibu Room”

**Prologue:** This forum will begin straight after the FENA annual review at the LUXE Hotel. The forum will be an intimate and informal get-together that aims to bring together PIs and sponsors aiming towards the one goal. This informal event will leverage time sponsors and PIs are all at the one place in Los Angeles. The first forum will focus on the Memory Showcase and the other will be based on the Nanopatterning Project Cluster. The respective PIs are expected to join and participate in the discussions.

**Expectations:** To engage industry and PIs to help guide their research for maximum benefit to PI research and applicability to the semiconductor industry. In addition, inputs into how memory concepts can be improved, integrated and developed will be discussed. Just in case, we ask that you have a simple slide that shows the operation and performance of your memory or patterning scheme to stimulate discussions if needed.

1.00pm	<b>Memory Showcase Forum</b>
1.00-3.30 pm	<p>1) What is current status/progress of the memory device. What is unique about this memory? In what way could this memory technology be superior to state of the art NAND &amp; DRAM?</p> <p>2) How can this technology be demonstrated and analyzed, i.e., what type of test chip is required for testing this memory technology &amp; what are the critical features of the test chip that are needed?</p> <p>3) How can the FENA program better assist with your goal?</p>
<b>3:30 – 4:00</b>	<b>Nanopatterning Project Cluster</b>
4.00 – 6.00	<p>1) What is current status/progress of this patterning technique? What is unique about this patterning technique? Ultimately, what is envisioned as the capability of this patterning technique (type of patterns attainable? How is this superior (or even complimentary) to state of the art DUV lithography and competing techniques such as Imprint litho?</p> <p>2) How can this technology be analyzed for it's suitability in large scale nanolithography? What critical resources are needed?</p> <p>3) How can the FENA program better assist with your progress?</p>
6.00pm	<b>Adjourn + Light Dinner</b>

**Out-take Comments by MICRON (something to think about):**

In the Table of FENA Memory Materials, we would like to see the latest ITRS numbers, including NAND flash. And beyond that, we believe it is beneficial to look at a few more parameters not listed that target more key parameters required of a good memory system. These include:

- Functional temperature range
- Minimum energy necessary for state transition on/off (This analysis may require some ab initio calculations)
- Estimation of signal to noise for the cell in a proposed architecture (this may help estimate potential for multi-level cell operation.)
- Read and Write Disturb characterization

-- Critical Roadblock(s) to commercialization (these need to be identified by Industry, which could start to be addressed at FENA forum)

A suggestion on the Nanopatterning side is to again identify the Critical roadblocks to getting these new patterning techniques to market. If the vision is that they will not be used with traditional CMOS integration, then roadmaps need to be developed to address new integration schemes and ways to implement. Additionally, Micron believes that for this FENA memory work to be successful, a **standardized test chip**, and list of test criteria, are required. We are willing to provide the layout (in GDSII format) for test modules to test: 1) the cell current for different electrode geometries, and 2) cell disturb characteristics for various cell spacings.