FENA

January 19-20, 2006
Santa Fe, New Mexico

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Computation in Nanoscale Dynamical Systems

a workshop on the promise and challenges
for computing in dynamical systems
of nanoscale electronic hardware

cellular automata
cellular nonlinear networks
random Boolean networks
complexity, emergent behavior
nanoscale cellular array architectures

Workshop on

Computation in Nanoscale Dynamical Systems

January 19-20, 2006
Bishop's Lodge Resort and Spa[†], Santa Fe, New Mexico

As part of the MARCO[*] Focus Center Research program, a workshop will be held to explore the potential of information processing in dynamical systems of nanoscale electronic hardware. Such **nanoscale dynamical systems (NDS)** include cellular automata implemented in large arrays of nanoscale components, as well as random Boolean networks and related paradigms based on less restrictive locality and regularity.

To set the stage, the theoretical development of **cellular automata (CA), random Boolean networks (RBN), and related paradigms** will be discussed together with software and hardware implementations. This includes implementation by conventional microprocessors and by custom chips for cellular nonlinear networks (CNNs), which can be viewed as generalized CA wherein local rules are updated and executed via a high-speed CMOS chip. Achieved milestones, limitations encountered in prior studies, and future promise will be discussed. Questions to be addressed include: What is the theoretical and experimental status of these approaches? To what classes of problems are they best suited? To what extent have useful methods for programming and design been developed? What specific computational tasks and killer applications exist for CA. How extendable are CA to general information processing tasks? In what ways do RBN and other more general paradigms enhance the picture; and what are the tradeoffs for hardware implementation?

With this foundation, the question of whether **nanoscale electronic hardware** based on massive arrays of ultrasmall components can enable the development of powerful NDS computing systems or subcomponents will be addressed. Proposed NDS circuitry includes locally connected arrays of simple nonlinear components (e.g., negative differential resistance elements) and of dynamical components (e.g., integrate-and-fire elements), which are capable of performing simple image processing tasks and memory. Questions concerning such systems include: Can the local communication and limited connectivity of CA, and certain RBN, alleviate the interconnect bottleneck and reduce power consumption? Can arrays of simple locally connected nonlinear components provide functions beyond basic image processing tasks? Can the richness of nonlinear dynamics compensate for the simplicity of nanoscale components? Do studies of nonlinear dynamics in the neocortex provide useful models for implementing NDS? Can these systems be made to work within limiting constraints imposed by lithographic resolutions, fine-grained regularity of self-assembly technologies, sustainable power-dissipation densities, low manufacturing yields and high error rates?

The workshop will also examine what the work on **complexity and emergent behavior** suggests for the ultimate capabilities of NDS: What role does array size play in determining the computational capabilities of these architectures; and what are the possibilities for realizing more intelligent systems with these paradigms?

The workshop will consist of invited talks, panels, and open discussion by participants from the fields of cellular automata, cellular nonlinear networks, random Boolean networks, and complexity who can relate their work to the development of NDS hardware for new information processing systems.

Please see www.fena.org for further details and registration & lodging information.

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[*]The Microelectronics Advanced Research Corp. (MARCO) funds and operates university-based research centers in microelectronics technology. (http://fcrp.src.org)

[†]Bishop's Lodge Resort and Spa. (http://www.bishopslodge.com/)

FURTHER BACKGROUND

Cellular Automata (CA) and Random Boolean Networks (RBN). Stephen Wolfram's recent book "A New Kind of Science" has intrigued technical people within and outside the community of cellular automata and stimulated increased interest in this field. The recent discovery of a universal 1D binary CA rule (Rule 110) is considered a theoretical milestone by many. However, Rule 110 is not efficient. Beyond its value as an "existence proof", are there any direct applications for 110 or the other recently discovered rules? More generally, what do the recent theoretical developments suggest for effective methods for finding rules and creating useful CA hardware? Stuart Kauffman's work on RBN has a wide range of implications in many fields. Do such networks, which can be viewed as generalized CA with relaxed restrictions on locality and regularity, offer significant advantages for computation? Is this relaxed locality and regularity compatible with practical hardware implementations.

Cellular Nonlinear Network (CNN) and Related Hardware. L. O. Chua's "standard" cellular nonlinear network is a mainly locally connected cellular array whose cells are continuous-time and continuous valued dynamical systems, and the interconnection weight patterns are also continuous valued. A large research community and body of work on this approach exist. Image processing with optical sensors in a 128x128 sensor and CNN processor array have been demonstrated. Cellular wave computers, based on the CNN universal machine (T. Roska and L.O. Chua), can implement an algorithmic sequence of templates and dynamics. What more can standard CNN and its extensions do? Which classes of problems can be handled? Is there a killer application for "information" processing (in contrast to "image" processing) for standard CNN implemented in CMOS?

Nanoscale Dynamical Systems (NDS). Nanoscale self-assembly methods offer the capability for arranging large numbers of ultrasmall elements into regular 2D arrays and more complex irregular patterns. Regularity (element type, size, and position) and structural simplicity (e.g., simple two-terminal nonlinear elements) ease the requirements for nanoscale manufacturing. Therefore, circuitry based on arrays of simple, locally connected nonlinear devices are well suited to the nanoscale. V. P. Roychowdhury and others have suggested circuitry for image processing and memory based on stationary patterns in 2D arrays. R. A. Kiehl and L. O. Chua have suggested the use of nonlinear dynamics, including chaotic modes, for novel spatial-temporal 2D image processing and memory. What is the potential of these and other types of nanoscale CNN? What range of image processing tasks and more general information processing tasks can they perform? What is the "low hanging fruit" for information processing and other applications? What types of high-level function could arise from emergent behavior in extremely large NDS?

A Reality Checklist for NDS Proposals. A number of issues should be kept in mind while assessing the promise of NDS proposals. What are the power requirements for the nanoscale devices, i.e., can one provide ultrascale functional densities under the constraints of sustainable power dissipation densities? What are the consequences of errors and the related overheads in terms of functional density? What are the patterning requirements? That is, if one needs random programming of the nanoscale devices, then one needs to address issues such as lithographic resolutions required to achieve such irregular designs, or propose directed self-assembly techniques. Where are the inputs and whether one needs to address nanoscale devices in the interior of the arrays to achieve functionality? How would power be delivered to the devices and what are the associated overheads? In general, it has been already shown that coupled circuits of non-linear devices are extremely powerful computational engines. But the challenge is to address the difficult issue of how to embed these systems efficiently in hardware, without losing the edge to implementations of the same systems on conventional digital computers.