Integrated Wafer-Scale Growth and Transfer of Directional Carbon Nanotubes and Misaligned-Carbon-Nanotube-Immune Logic Structures


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Abstract

We successfully demonstrate essential components and their integration for large-scale Carbon Nanotube Field Effect Transistor (CNFET) technology: 1. First demonstration of full-wafer-scale growth of directional carbon nanotubes (CNTs) on 4" single-crystal quartz wafers. 2. First demonstration of full-wafer-scale CNT transfer from 4" quartz wafers to 4" silicon wafers for integration on silicon. 3. Integration of full-wafer-scale growth and transfer, together with metallic-CNT removal, for the first demonstration of misaligned-CNT-immune digital logic structures on a full-wafer-scale. Such logic structures guarantee correct logic functionality in the presence of a large number of misaligned and mis-positioned CNTs.

Introduction

Carbon Nanotube Field Effect Transistors (CNFETs) are promising extensions to silicon CMOS, and can provide 13X improvement in Energy-Delay product over 32 nm CMOS [1]. Despite major progress, e.g., ring oscillator using a single CNT [2], significant research is needed for design and integration of VLSI CNFET circuits. Essential components for such large-scale integration are: 1. Full-wafer-scale directional CNT growth (CNTs refer to Single-Walled CNTs): Full-wafer-scale CNT growth enables fabrication of CNFET circuits in mass scale using conventional lithography. CNTs grown on ST-cut quartz are significantly better aligned compared to silicon [3] or r-plane sapphire [4] for comparable CNT densities. Unfortunately, existing CNT growth techniques on quartz (e.g., [5]) do not allow such full-wafer-scale CNT growth; 2. Full-wafer-scale CNT Transfer: Large-scale silicon integration requires full-wafer-scale transfer of directional CNTs from quartz to silicon substrates; and, 3. VLSI-compatible Imperfection-Immune CNFET Circuits: Perfect alignment and positioning of all CNTs cannot be guaranteed at VLSI scale. Misaligned- and mis-positioned-CNT-immune logic structures, designed using principles described in [6], are required. However, such logic structures have not been experimentally demonstrated. CNFETs require semiconducting-CNTs. Metallic-CNTs create source-drain shorts and require removal using burning [7] or selective etching [8]. This paper successfully demonstrates the above essential components and their integration for large-scale CNFET circuits. We provide data on a large number of devices (cross-chip, cross-wafer) to illustrate the variability of process/device parameters relevant for VLSI integration consideration.

Wafer-Scale Directional CNT Growth on Quartz

High temperature (850°C) is required for growing directional CNTs [5]. CNT growth on quartz has only been demonstrated for wafer pieces because the transformation from alpha to beta quartz at ~573°C results in wafer fracture during ramp-up [9]. The key to achieving full-wafer-scale directional CNT growth is to control the temperature ramp rate near the phase transformation temperature (550°C – 620°C) to < 1°C / min (Fig. 1a). Unpatterned Ferritin was used as a catalyst for CNT growth. Prior to growth, the quartz wafer was annealed for 8 hrs in oxygen at 900°C using controlled ramp rate similar to Fig. 1a. Figs. 1b-e demonstrate that our new technique enables full-wafer-scale CNT growth on 4" quartz wafers. Fig. 1e also demonstrates that CNTs grew across the entire wafer with >94% of the measured devices being functional. The reproducibility of this technique is confirmed by multiple full-wafer-scale growth runs for various experiments presented in this paper. As shown in Fig. 2a, CNT alignment can be significantly improved by patterning the catalyst (similar to [10]).

Wafer-Scale CNT Transfer and CNFET Fabrication

Next, we demonstrate a new technique for full-wafer-scale CNT transfer from quartz to silicon for large-scale silicon integration. Previous CNT transfer techniques, e.g., [11, 12], did not demonstrate full-wafer scale transfer. Figs. 3a-f show the sequence of CNT transfer steps using thermal release tape. This low-temperature (120°C) technique preserves CNT directionality (Fig. 3e). Fig. 3g demonstrates that CNTs were successfully transferred across the entire wafer with >92% of the measured CNFETs being functional.

Metallic-CNT removal is essential for CNFET circuits. We applied electrical burning [7] to burn metallic-CNTs in CNFETs after full-wafer-scale transfer. Electrical burning is performed by applying high V_{ds} while turning off semiconducting CNTs using the gate. Metallic CNTs pass high current and are burnt resulting in improved I_{on}/I_{off} ratios of 10^4 – 10^5 (Figs. 4a, b). CNFETs retain well-behaved I-V characteristics after electrical burning (Fig. 4c).

Misaligned- and Mis-positioned-CNT-Immune Logic Structures

It is nearly impossible to guarantee perfect alignment and positioning of all CNTs at VLSI scale. This can result in incorrect logic behaviors of fabricated logic structures (Fig. 5). In [6], we developed design principles for CNFET circuits that guarantee correct logic functions in the presence of a large number of misaligned and mis-positioned CNTs. For example, for a NAND pull-up, during layout design, we identify a lithographically-defined region from where CNTs are etched out (Fig. 6). Any structure consisting exclusively of series-connected CNFETs, e.g., NOR pull-up or NAND pull-down, is inherently immune to misaligned and mis-placed CNTs. The special layout design technique can be applied to any logic function, and is compatible with VLSI, i.e., it does not require special customization on individual die basis.

We present first experimental demonstration of misaligned-CNT-immune logic structures on both quartz after full-wafer-scale CNT growth (Fig. 7) and silicon after transfer of CNTs from quartz to silicon (Fig. 8). These logic structures correspond to pull-ups of NAND, NOR, AND-OR-INVERT and OR-AND-INVERT functions. For example, consider the NAND pull-up on quartz (Fig. 7a) and silicon (Figs. 8a-c). When both gates are off, the drive current (I_{drive}) is minimum. When both gates are on, I_{drive} is maximum, and when only one of the gates is on, I_{drive} is approximately halfway between minimum and maximum. Minimum I_{drive} is non-zero due to metallic-CNTs (metallic-CNTs also cause leakage in the NOR pull-up of Fig. 7b). To overcome this, we removed metallic-CNTs using electrical burning after fabrication of misaligned-CNT-immune logic structures. Fig. 9 demonstrates correct behavior of a misaligned-CNT-immune NAND pull-up on silicon after electrical burning of metallic-CNTs. In this case, when both the gates are off, the I_{drive} is very small. The I_{on}/I_{off} ratio is > 10^6, and well-behaved I-V characteristics are obtained.

Conclusion

Full-wafer-scale CNT growth on quartz, full-wafer-scale CNT transfer from quartz to silicon, their integration with metallic-CNT removal, and demonstration of misaligned-CNT-immune logic structures pave the way for VLSI CNFET technologies. It may be possible to integrate such an approach with silicon CMOS. For performance benefits of CNFETs over CMOS, the following open issues must be resolved: 1. High CNT density: One potential technique is to perform wafer-scale CNT transfer (Fig. 3) multiple times from multiple quartz wafers to the same target silicon wafer; 2. Scalable metallic-CNT removal [8]; and, 3. Metallic-CNT-tolerant circuits [13].

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References

Figure 1. (a) Time course of full-wafer-scale CNT growth on 4" quartz wafers. (b) 4" quartz wafer after CNT growth and contact definition [Ti(1 nm)/Au(50 nm)]. (c) Aligned CNTs bridging two contacts. (d) SEM images of CNTs in five regions of the wafer. CNT density is ~2 CNTs/µm. Scale bars are 20 µm. (e) Current distributions at 1V. (f) Current (I) vs. Drain current (Vds) for CNTs at predefined during layout design. (g) Etch CNTs from regions predefined during layout design. **In the experimental demonstrations (Fig. 8-10), CNTs are inherently p-doped.**

Figure 2. (a) CNT growth on quartz using 0.2 nm Fe catalyst in lithographically defined regions. (b) Zoomed inset from Fig. 2a. (c) CNT diameter distribution.

Figure 3. CNT transfer technique using Thermal Release Tape. (a) SEM of CNTs on quartz. (b) 100 nm of Au evaporated on 4" quartz wafer after CNT growth. (c) Thermal release tape is applied to the Au film and the tape/Au bilayer is peeled off. (d) SiO2/Si Wafer with transferred Au after tape release at 120°C. (e) SEM images of SWNTs transferred from quartz to 50 nm SiO2 on Si at gold etching (KJ1). (f) Si wafer after substrate-gated CNFET fabrication. (g) Current distributions (Vgs = 1V Vdd = -5V) for n (out of 18 in each die) functional CNFETs (W=50 µm, L=1 µm, tsox=50 nm, T=5 nm)/Au(50 nm) contacts in 5 arbitrary dies (of 133) in 5 regions of the wafer.

Figure 4. (a) CNFET current-voltage (Ids vs. Vds) before and after metallic-CNT burning (W=10 µm, L=1 µm, tsox=50 nm). (b) Electrical burning of metallic CNTs improves Ids/Ioff ratio to 10^4. (c) Ids vs. Vds after burning for another CNFET.

Figure 5. Incorrect Logic Functionality in the presence of misaligned CNTs.

Figure 6. Misaligned-CNT-immune circuits using top-gated CNFETs. (a) Cross-section. (b) CNFET SEM. (c) Misaligned-CNT-immune NAND pull-up. (d) Misaligned-CNT-immune NAND pull-up after etching. (e) Process steps.

Figure 7. Misaligned-CNT-immune logic structures on quartz after full-wafer-scale CNT growth without metallic-CNT burning. NAND pull-up (a) and NOR pull-up (b) with SEM images and drive currents for all on/off input combinations. Contacts and Gate Metal: Ti(1 nm)/Au(50 nm), Gate dielectric: 10 nm H2O.

Figure 8. Misaligned-CNT-immune logic structures on silicon after CNT transfer and without metallic-CNT burning. (a)-(c) NAND pull-up. (d) AND-OR-INVERT pull-up and (e) OR-AND-INVERT pull-up logic structures and SEM images.

Figure 9. Misaligned-CNT-immune NAND pull-up on silicon after CNT transfer and metallic-CNT burning. Leakage currents are extremely small. Contacts and Gate Metal: Ti (1 nm)/Pd (50 nm), Gate dielectric: 50 nm H2O. (thick oxide needed to prevent oxide breakdown during metallic-CNT burning).